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P O BOX 655474, M/S 3999
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 33

Application Number: 08/890,894
Filing Date: July 10, 1997
Appellant(s): CHAUVEL ET AL.

Ronald O. Neerings
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/16/02.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

The statement of the status of the claims contained in the brief is correct.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant□s statement of the issues in the brief is substantially correct. The changes are as follows: 5) Are claims 34 and 37-39 patentable under 35 U.S. C. 1039a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, further in view of Finch et al., U.S. Patent No. 4,783, 778? Claim 35 was not rejected under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035 in view of Asano et al., U.S. Patent No. 5,237,686, further in view of Finch et al., U.S. Patent No. 4,783, 778.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 6-15, 17, and 34-39 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

A substantially correct copy of appealed claim 17 appears on page 2 of the Appendix to the appellant's brief. The minor errors are as follows: "The Asano reference . . . of claim 6" should not in claim 17.

(9) Prior Art of Record

4,783,778	Finch et al.	11-1998
4964035	Aoyama et al.	10-1990
5,237,686	Asano et al.	8-93
5210861	Shimoda	5-93

Morris Mano, Computer System Architecture, 1982, pages 264, 282-283, and 502

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 36-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Finch et al., US Patent No. 4783778, hereinafter Finch.

As per **claims 36-39**, Finch teaches the invention as claimed, an apparatus comprising: a first processor or **a protocol processor (e.g., fig.1, B processor) where the first processor being suited to execute tasks to which a main processor is not suited (e.g., B processor performing x.25 protocol processing, col. 14, line 48 and**

A processor controlling mini packet protocol, Netlink protocols, initialization, col. 8, line 31 and et seq.), comprising a core (e.g., fig.1, el. 65sc102), **a program memory (e.g., col. 14, line 22 and et seq. or col. 8, line 38 and et seq.)**, and a local memory (e.g., fig. 1, buffer of B processor or col. 6, line 62 and et seq.)**; a second processor or the main processor (e.g., fig.1, A processor; and col.8, line 36 and et seq.), where the second processor, of a design other than the first processor (e.g., fig. 1, A processor comprising: ROM and mini packet receiver/ transmitter (MPRT), of a design other than B processor having protocol serial controller (MPSC) and baud rate generation circuit)**, comprising a core (e.g., fig.1, el. 65sc102), **a program memory (e.g., fig.1, ROM)**, and a local memory (e.g., fig.1, RAM of A processor); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, col. 8, line 55 and et seq.; or fig.1, el. common memory interface and control); and one and only one common memory coupling the local memory of the first processor to the local memory of the second processor (e.g., fig.1, common memory).

2. Claims 6-7, 9-15, 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (hereinafter Aoyama) in view of Asano et al., U.S. Patent No. 5237686, (hereinafter Asano). The rejections are maintained set forth in the previous Office action.

As per **claims 6 and 36**, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600),

comprising a core (e.g., fig.1, el. 601); a second processor for performing vector processing, of **a design other than the first processor (e.g., fig. 1, el. 500, vector processor)**, comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory circuit for coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though **Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.)**. Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. **Asano** (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having **a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory** are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing

speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

As per **claim 7**, Aoyama shows the use of the second processor being a main processor (e.g., col.4, line 63 and et seq.).

As per **claim 9**, Aoyama does not specifically show the second processor as a DSP. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality.

As per **claims 10-13**, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM. Asano (e.g., figs. 1-2, els 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama

and Asano do not explicitly show a program memory as a ROM. Official Notice is taken that both the concept and advantages of providing; a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to loose data when power is removed from it.

As per **claims 14, 15, and 17**, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig.1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g., cols. 5-6). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of

Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

3. Claims 8 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Morris Mano, Computer System architecture, 1982, pages 264 and 282-283, (hereinafter Mano).

As per **claim 8**, Aoyama does not specifically show the scalar processor as a microprocessor. Mano, page 264, line 8 and et seq., is cited merely as an example to show both the concept and advantages of providing a processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a processor into a microprocessor to Aoyama because it would provide for a reduction in space and signal lines between functional elements, leading to an increase in processing performance, and a low cost.

As per **claim 35**, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of vector processing including signal processing tasks generally carrying out by a DSP and matrix computation performed by an array processor. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and

advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Mano, e.g., page 282 line 36 and et seq., has been cited as an example to show that both the concept and advantages of providing vector processing including the use of array processor for performing matrix computations are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an array processor performing array computations into Aoyama because it would allow parallel computations on large arrays to be performed, thereby, increasing system computation power.

4 Claims 34-35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of applicants admitted prior art, Background of the invention, the instant specification page 1 line 6 to page 2, line 11, (hereinafter AAPA).

As per **claims 34-35**, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is

the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Also, AAPA, the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing or a protocol processor; and vector processing including the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

As per **claims 37-39**, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing of a design other than a

main processor (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601) where the first processor being suited to execute tasks to which a main processor is not suited; a second processor or the main processor (e.g., col.4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase

processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. AAPA, the instant specification page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing because it would allow protocol processing to be performed; thereby, increasing system functionality.

5. Claims 34 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Finch et al., U.S. Patent No. 4783778, (hereinafter Finch).

As per **claim 34**, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els. 500 and 600 and cols. 2, line 5 and et seq.); and the scalar processor (e.g., fig. 1., els. 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing. Finch, e.g., col. 8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing or protocol processor are

well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

As per **claims 37-39**, Aoyama teaches the invention substantially as claimed, comprising: a first processor (e.g., fig.1, el. 600) for performing scalar processing, of a design other than a main processor or of a design which enables the processor to execute tasks, where the first processor being suited to execute tasks to which a main processor is not suited, comprising a core (e.g., fig.1, el. 601) ; a second processor or the main processor (e.g., col.4, line 63 and et seq.); for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of

each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. Finch, e.g., col.8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

(11) Response to Argument

Applicant's arguments filed 12-16-02 have been fully considered but they are not persuasive.

1. In the appellant argument, the appellant argued (1) that Finch's B processor did not have a program memory as required by claims 36-39 and fig.1 showed that there was no program memory in the B processor or none of the memory was within the B processor.

As to point (1) the examiner disagreed with the appellant's arguments. In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., program memory **in** the B processor or none of the memory was **within** the B processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What the claims do however state is "comprising". The above claimed limitation "comprising" is taught by Finch as described below.

The examiner disagrees with the appellant's arguments because Finch teaches the B processor **comprising** a program memory (fig. 1, common memory RAM, local to "B" and col. 8, lines 37-41) **as recited in the claims 36-39**. Even though, the common memory, RAM local to "B" is not within the B processor physically, it is still the program memory of the B processor because it is accessible to the B processor and it stores software for execution by the B processor (e.g. col. 8, lines 37-41). Since the common memory, RAM local to "B" stores software for execution of the B processor and it is the memory of the B processor, then it is a part (i.e., comprising) of the B processor and it is in B logically.

2. In the appellant argument, the appellant argued (2) that Finch fails to teach a **second processor, of a design other than the first processor**, comprising: a core, a **program memory**, and a local memory, as required by claim 36 or **a protocol processor, of a design other than said main processor,** comprising a core, **a program memory**, and a local memory as required by claim 37, or a protocol processor, comprising a core, **a program memory**, and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited, as required by claim 38, or a **protocol processor** comprising a core, **a program memory** and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited as required by claim 39 (Appeal Brief filed 12/16/02 page 15, paragraph 1) .

As to point (2) the examiner disagrees with the appellant's arguments. Finch teaches the invention as claimed, an apparatus comprising: a first processor or a **protocol processor** (e.g., fig.1, B processor) **where the first processor being suited to execute tasks to which a main processor is not suited** (e.g., B processor performing x.25 protocol processing, col. 14, line 48 and A processor controlling mini packet protocol; Netlink protocols, initialization, col. 8, line 31 and et seq.), comprising a core (e.g., fig.1, el. 65sc102), **a program memory** (e.g., col. 14, line 22 and et seq. or col. 8, line 38 and et seq.), and a local memory (e.g., fig. 1, buffer of B processor or col. 6, line 62 and et seq.)**; a second processor or the main processor** (e.g., fig.1, A processor; and col.8, line 36 and et seq.), where the second processor, **of a design**

other than the first processor (e.g., fig. 1), a processor comprising: ROM and mini packet receiver/ transmitter (MPRT), of a design other than B processor having protocol serial controller (MPSC) and baud rate generation circuit), comprising a core (e.g., fig.1, el. 65sc102), **a program memory (e.g., fig.1, ROM)**, and a local memory (e.g., fig.1, RAM of A processor).

3. In the appellant argument, the appellant argued (3) that it would not have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Asano which discloses processors for vector processing into Aoyama which discloses one processor for scalar processing and one for vector processing. Also, answer to the response to Examiner 's rebuttals (10) (Appeal Brief filed 12/16/02 page 17) .

As to point (3) even though Asano teaches vector processors and Aoyama teaches a vector processor and a scalar processor, both of the references teach controlling a plurality of processors for accessing a common memory. Therefore, the examiner would apply the teaching of each processor comprising ROM, a RAM (e.g., Asano, fig. 1, els 22-23) and one and only one common memory (e.g., Asano, fig.17 and 6, els. 62 , 172 and fig. 1, el. 14a coupling the processors to a common memory 1). The examiner disagrees with the appellant's arguments because Aoyama teaches the use of controlling a plurality of processors to access a common memory (e.g., col. 5, lines 1-10), and Asano discloses the same subject matters (e.g., fig.6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61). It

would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. In further discussion, the examiner would apply the teaching of Asano as discussed above to modify the Aoyama but would not physically combine the two systems together. Basically, the feature is very well known in any type of computer architecture field. The examiner is simply choosing one of many to use as an example, to show Appellant's claimed features.

4. In the appellant argument, the appellant argued (4) that Asano fails to teach or suggests a "synchronizing circuit for coupling the core of said first processor to the core of said second processor," as required by claims 6 and 36.

As to point (4) the examiner disagrees with the appellant's arguments. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Even though the examiner used Aoyama to show the use of the synchronizing circuit (e.g., fig. 1, els. 810 or 800a, col. 5, lines 1-10), also, Asano clearly teaches or

suggests a synchronizing circuit for coupling the core of said first processor to the core of said second processor (e.g., col. 10, lines 15-30; fig.6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61;). It does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second processor because Aoyama teaches the feature as stated in the rejection above.

In further discussion, with respect to claim 36, In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which applicant relies (i.e., synchronizing circuit for coupling **the core of** said first processor to **the core of** said second processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. In the appellant argument, the appellant argued (5) that Asano failed to teach "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor," as required by claim 36; since Asano discloses "multiple" common memories. Also, answer to response to examiner rebuttal (13) (Appeal Brief filed 12-16-02, page 22).

As to point (5) the examiner disagrees with the appellant's arguments. In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which applicant relies (i.e.,

coupling **the local memory of** the first processor to **the local memory of** the second processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Asano clearly discloses one and only one common memory coupling **said first processor to said second processor**," as recited in the claim 36 (e.g., fig.6, a common memory 62; and col. 12, lines 53-61; fig. 1, el. 14a coupling the processors to a common memory 1, or figs.6 and 17, els.62, one and only one common memory 172 couple to processor 173a-173b and local memories 174a-174b).

Asano, fig. 1 not only teaches "multiple common memories," but also shows at a specific time "one and only one common memory" of the multiple common memories coupled to the requesting processors, while the other memory busses coupled to the other common memories are idle (e.g., col. 12, lines 3-15). In particular, fig. 1, Asano shows processor modules 11a and 11b coupling to a memory 9 by memory bus 3; processor modules 11a and 11b coupling to a common memory 1 or el. 10a; and processor modules 11a and 11b coupling to a common memory n by memory bus 14n. Furthermore, Asano, fig. 1 and col. 12, lines 3-15, shows at some specific time, only the modules processor 11a and 11b request access to the common memory 1 or 10a while the other processor modules do not need to access other common memories, one and only one common memory 1 or 10a couples the processor module 11a to processor module 11b while the other memory buses are idle. Therefore, Asano, fig. 1,

shows "one and only one common memory coupling the first processor to the second processor."

In further discussion, assuming "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor" is required by claim 36. Asano, fig. 17 shows one and only one common memory 172 coupling the local memory 174a of the processor 173a to the local memories 174b of the processor 173b ; and fig. 1 and col. 12, lines 3-15 as discussed above. As shown above at a specific time one and only one common memory of the plurality of common memories coupling the first processor modules to the second processor module wherein a local memory (e.g., fig. 2, RAM 22, buffers) is inside each of the processor modules. Therefore, Asano, figs. 17 and 1- 2, also, shows "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor."

6. In the appellant's argument, appellant argued (6) that nothing in the examiner 's reference to fig. 1 or fig. 6, shows a common memory coupling the local memory of a first processor to another memory of a second processor because Asano processors are already coupled to each other and memory 62 does not couple one processor to another.

As to point (6) the examiner disagrees with the appellant's arguments because Asano teaches many different ways for coupling the local memory of the first processor to the local memory of the second processor (e.g., fig. 17, coupling by only memory bus

or coupling by the common memory 172 and memory bus). Fig. 17, Asano shows a common memory 172 and the bus 176 coupling a local memory 174a of processor 1 to a local memory 174b of processor 2. In particular, fig. 17, Asano shows coupling data from the local memory 174a of the first processor to the common memory (e.g., col. 2, lines 15-20) and coupling data from the common memory to the local memory 174b of the second processor (e.g., col. 2, lines 5-10). Fig. 1, Asano shows a common memory 1 or 10a coupling the processor module 11a to a processor module 11b via a memory bus 14a. According to figs. 1-2, when the processor 11a request to write data from its local memory to the common memory 10a, there is coupling data from the local memory to the common memory 10a. When the processor 11b request for reading data from the common memory 10a, there is coupling data from the common memory to the local memory of the processor 11b. Therefore, Asano, figs. 17 and 1, shows one and only one common memory circuit coupling the local memory of the first processor to the local memory of the second processor.

7. In the Appellant's argument, Appellant argued (7) that Shimoda did not teach the use of having data from a local cache 3A instead of having data from a common memory 7c every time to increase processing speed (Appeal Brief filed 12-16-02, page18, first and second paragraphs)

As to point (7) the examiner disagreed with the appellant's arguments. Shimoda, col. 3, lines 20-30, teaches "The S-unit 3A (3B) constitutes a cache memory system and includes . . . an internal memory , , , 5A (5B) . . . where **data** designated by the I unit 2A

(2B) is **present in the storage 5A** (5B), the S-unit **accesses to the storage 5A** (5B), and **when the data is not present, the S-unit 3a 3(B) directly accesses to the common memory 7c . . .**" As seen from fig.1, the location of the local memory cache 3A is closer to the I unit than the common memory 7c, processing data from the local memory cache 3A is faster than processing data from the common memory 7c; therefore, increase processing speed. These are the basics for memory hierarchy and principle of locality.

8. In the Appellant's argument, Appellant argued (8) that Shimoda and Morris Mano fail to provide any additional teaching it would increase processing speed of each processor by having local memories and program memories instead of a main memory, thereby increasing the processing efficiency for each processor (Appeal Brief filed 12/16/02, page19, first and second paragraphs)

As to point (8) the examiner disagrees with the appellant's arguments. Shimoda, col. 3, lines 20-30, teaches "The S-unit 3A (3B) constitutes a cache memory system and includes . . . an internal memory , , , 5A (5B) . . . where **data** designated by the I unit 2A (2B) is **present in the storage 5A** (5B), the S-unit **accesses the storage 5A** (5B), and **when the data is not present, the S-unit 3a 3(B) directly accesses to the common memory 7c . . .**" As seen from fig.1, the location of the local memory cache 3A closer to the I unit than the common memory 7c, processing data from the local memory cache 3A is faster than processing data from the common memory 7c; therefore, increase processing speed. These are the basics for memory hierarchy and principle of locality.

Also, Morris Mano, pages 502, lines 13-14 shows the use of accessing a cache memory instead of accessing a main memory every time requested data to increase speed processing of a processor .

9. In the Appellant's argument, Appellant argued (9) that it does matter whether or not Asano teaches a synchronizing circuit for coupling the core of said first processor to said core of said second processor because "it goes to the core of whether or not one of ordinary skill in the art at the time the invention would have been motivated to combine the two teachings . . . had been determined (Appeal Brief filed 12/16/02, page 21, first paragraph to page 22, first paragraph)

As to point (9) the examiner disagrees with the appellant's arguments. As stated in the rejections, the rejection based on the combination of Aoyama and Asano. Even though the examiner used Aoyama to show the use of the synchronizing circuit (e.g., fig. 1, els. 810 or 800a, col. 5, lines 1-10), also, Asano clearly teaches or suggests a synchronizing circuit for coupling the core of said first processor to the core of said second processor (e.g., col. 10, lines 15-30; fig.6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61;). It does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second processor because Aoyama teaches the feature as stated in the rejection above.

Also, as stated in the rejections above, the examiner motivation to combine the Asano reference to the system of Aoyama based on the teaching of a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory but not a synchronizing circuit.

10. In the Appellant's argument, Appellant argued (10) that the examiner has not satisfied the first, second, and third requirements to establish a prima facie case of obviousness in rejecting claims 6 and 36.

As to point (10) the examiner disagrees with the appellant's arguments. It is noted that motivation is clearly expressed in the rejections. Clearly a reasonable expectation of success exists. And "All" the claimed limitations have been met as discussed in the rejections.

11. In the Appellant's argument, Appellant argued (11) that the examiner provides no teaching from the prior art that indicates that the teaching of Asano can be combined with Aoyama in order to modify Aoyama, with any hope of success (Appeal Brief file 12-16-02, page 17, paragraph 2).

As to point (11) the examiner disagrees with the appellant's arguments. As noted from the appellant page 23, paragraph 1, " there must be some suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In this case, It would have been obvious to one of

ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Shimoda, col. 3, lines 20-30, teaches "The S-unit 3A (3B) constitutes a cache memory system and includes . . . an internal memory , , , 5A (5B) . . . where **data** designated by the I unit 2A (2B) is **present in the storage 5A** (5B), the S-unit **accesses to the storage 5A** (5B), and **where the data is not present, the S-unit 3a 3(B) directly accesses to the common memory 7c . . .**" As seen from fig.1, the location of the local memory cache 3A closer to the I unit than the common memory 7c, processing data from the local memory cache 3A is faster than processing data from the common memory 7c; therefore, increase processing speed.

Also, Morris Mano, pages 502, lines 13-14 shows the use of accessing a cache memory instead of accessing a main memory every time requested data to increase speed processing of a processor .

12. In the Appellant's argument, Appellant argued (12) that Aoyama fail to teach or suggest the main processor with processors DMM1-DMMk (Appeal Brief page 23, paragraphs 3 and 4).

As to point (12) the examiner disagrees with the appellant's arguments. In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which applicant relies (i.e., with processors DMM1-DMMk) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further more, Aoyama teaches or suggests wherein the second processor is the main processor of the apparatus. For example, "the vector processing system," col. 4, and line 63. Because the vector processing is a main processing in the system, it is called the **vector processing system** but not a scalar- vector processing system or a scalar processing system. Since the vector processor performs the main processing, it is the main processor of the vector processing system.

13. In the appellant argument, the appellant argued (13) Aoyama and Asano fail to teach or suggest wherein the second processor is a DSP.

As to point (11) the examiner disagrees with the appellant's arguments. Asano (e.g., col. 1, line 16 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art.

14. In the remarks, the applicant argued (12) Aoyama and Asano fail to teach or suggest the use of RAM and ROM.

As to point (12) the examiner disagrees with the applicant's arguments. Asano (e.g., figs. 1-2, els. 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, for teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show a program memory as a ROM. Official Notice was taken that both the concept and advantages of providing a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to loose data when power is removed.

15. In the appellant argument, the appellant argued (15) with respect to claims 10-13 that "the examiner relied upon his own experience and motivation for citing the obviousness of the above additional limitations. The Examiner should cite prior art to support his position." (Appeal Brief filed, page 24, paragraph 7th.)

As to point (15) the examiner disagrees with the appellant's arguments. The examiner is unclear which portion of the rejections the appellant is referring to. The well known in the art statement is taken to be admitted prior art because appellant failed to seasonably traverse the examiner 's assertion of the official notice. The examiner cited all prior art that she needs to.

16. In the appellant argument, the appellant argued (16) that Aoyama and Asano fail to teach or suggest wherein the memory circuit for coupling the local memory of the first to the local memory of the second processor being physically separate from the first and second processors.

As to point (16) the examiner disagrees with the appellant's arguments. Aoyama teaches the memory circuit for coupling the local buffer of the first processor to the local register of the second processor being physically separate from the first and second processors (e.g., fig.1, el. 800). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program

memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

17. In the appellant argument, the appellant argued (17) with respect to claim 14 that the examiner is improper relying upon hindsight reconstruction and the motivation for the combination comes from the Examiner- Not from the prior art

As to point (17) the examiner disagrees with the appellant's arguments. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

As noted from the appellant page 23, paragraph 1, " there must be some suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In this case, It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory

for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Shimoda, col. 3, lines 20-30, teaches "The S-unit 3A (3B) constitutes a cache memory system and includes . . . an internal memory , , , 5A (5B) . . . where **data** designated by the I unit 2A (2B) is **present in the storage 5A** (5B), the S-unit **accesses to the storage 5A** (5B), and **where the data is not present, the S-unit 3a 3(B) directly accesses to the common memory 7c . . .**" As seen from fig.1, the location of the local memory cache 3A closer to the I unit than the common memory 7c, processing data from the local memory cache 3A is faster than processing data from the common memory 7c; therefore, increase processing speed.

Also, Morris Mano, pages 502, lines 13-14 shows the use of accessing a cache memory instead of accessing a main memory every time requested data to increase speed processing of a processor .

18. In the appellant argument, the appellant argued (18) Aoyama and Asano fail to teach or suggest wherein the memory circuit coupling the local memory of the first processor to the local memory of the second processor is a DPRAM memory

As to point (18) the examiner disagrees with the appellant's arguments. Aoyama teaches the memory circuit coupling the local buffer of the first processor to the local register of the second processor is a DPRAM memory (e.g., col. 10, line 15, RAM 108;

and fig. 5, RAM 108 with dual ports. Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

19. In the appellant argument, the appellant argued (19) that Aoyama did not describe a common memory.

As to point (19) the examiner disagrees with the appellant's arguments. Aoyama fig. 1 and abstract, line 16, show a common memory 800a, a logical partition of the common memory and fig. 5, shows **a** common memory **circuit** 108-1 as recited in claim 6.

20. In the remarks, the appellant argued (20) Aoyama and Asano fail to teach or suggest wherein the synchronizing circuit ensure that only one of the processors utilized the memory circuit for coupling the local memory of the first processor to the local memory of the second processor, at any one.

As to point (20) the examiner disagrees with the appellant's arguments. Aoyama teaches wherein the synchronizing circuit ensure that only one of the processors utilize the memory circuit for coupling the local buffer of the first processor to the local register of the second processor, at any one time (e.g., col. 5, line 63 and et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each

processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Also, Aoyama (e.g., col. 5, lines 63 and et seq.) teaches the use of flip flop circuits (a circuit that changes between two possible states when a pulse is receive at the input) indicating an access to the common memory based on a pulse or timing and the use of the test and lock processing (i.e., TAS) where in light of the appellant's specification line 7, lines 35-36 stated "signals TAS which are intended for synchronization".

21. In the appellant argument, the appellant argued (21) that the Examiner has not satisfied the above requirements in rejecting claims 8 and 35.

As to point (21) the examiner disagrees with the appellant's arguments. It is noted that the motivation is clearly expressed in the rejections. Clearly a reasonable expectation of success exists. And "All" the claimed limitations have been met as discussed in the rejections.

22. In the appellant argument, the appellant argued (22) with claim 34, AAPA does nothing to overcome the above-identified deficiencies of the Aoyama and Asano, nor is there any teaching of the combination of AAPA with the teaching of Aoyama and Asano.

As to point (22) in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the

claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, AAPA, the instant specification, e.g., page 1 line 13 to line 18, teaches "scalar processing encompasses a high level task which is the monitoring of the application or the management of functioning and tasks which are generally carried out by hardwired logic or a processor which may be identified as protocol processing" or protocol processor well known in the art and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality.

23 In the appellant argument, the appellant argued (23) with claim 35 that Aoyama and Asano fail to teach of suggest "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP an the use of array processor type".

As to point (23), in response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which applicant relies (i.e., "the use of scalar processing encompassed in a high level task which is the monitoring of an application") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The combination of Aoyama, Asano, and AAPA teaches vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type as recited in claim 35.

In particular, Aoyama teaches vector processing (e.g., abstract); Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Also, AAPA, of the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of vector processing including the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

24. In the appellant argument, the appellant argued (24) with claim 35, AAPA does nothing to overcome the above-identified deficiencies of the Aoyama and Asano, nor is there any teaching of the combination of AAPA with the teaching of Aoyama and Asano..

As to point (24) in response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the instant specification, e.g., page 1 line 13 to line 18, teaches "vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which required a more powerful structure than that of the DSP and which is generally of the 'array processor ' type." The use of vector processing including an array processor type is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

25. In the appellant argument, the appellant argued (25) that Asano failed to teach "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor," as required by claims 37 and 39, since Asano discloses "multiple" common memories.

As to point (25), Asano, fig. 1 not only teaches "multiple common memories," but also shows at a specific time "one and only one common memory" of the multiple common memories couple the requesting processors, when the other memory busses are coupled to the other common memories and are idle (e.g., col. 12, lines 3-15). In particular, fig. 1, Asano shows processor modules 11a and 11b coupled to a memory 9 by memory bus 3; processors modules 11a and 11b coupled to a common memory 1 or el. 10a; and processor modules 11a and 11b coupled to a common memory n by memory bus 14n. Further more, Asano, fig. 1 and col. 12, lines 3-15, shows at some specific time, if only the modules processor 11a and 11b request to the common memory 1 or 10a while the other processor modules do not need access to other common memories, one and only one common memory 1 or 10a couples the processor module 11a to processor module 11b while the other memory buses are idle. Therefore, Asano, fig. 1, shows "one and only one common memory coupling the first processor to the second processor."

In further discussion, regarding to "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor" is required by claims 37 and 39. Asano, fig. 17 shows one and only one common memory 172 coupling the local memory 174a of the processor 173a to the local memories 174b

of the processor 173b ; and as discussed above, fig. 1 and col. 12, lines 3-15 teach at a specific time one and only one common memory of the plurality of common memories coupling the first processor modules to the second processor module wherein a local memory (e.g., fig. 2, RAM 22, buffers) is inside each of the processor modules. Therefore, Asano, figs. 17 and 1- 2, also, shows "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor."

26 In the remarks, the applicant argued (26) that the examiner has provided no evidence to support her determination (i.e., it would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality).

As to point (25) the examiner disagrees. The examiner has provided evidence to support her determination. AAPA states that protocol processing is generally carried out by the use of a scalar processor, as shown above. Aoyama shows the use of a scalar processor. AAPA adds functionality to a scalar processor (i.e., the protocol processor performs protocol processing). Therefore the evidence is the reliance of AAPA.

As noted from the appellant page 31, last paragraph to page 32, " there must be some suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In this case, it would have been obvious to one of ordinary skill in the art to include a protocol processor performing

protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

27. In the appellant argument, the appellant argued (27) the three basic criteria must be met (i.e., suggestion or motivation to combine the references, reasonably expectation of success and must teach or suggest ALL the claim limitations).

As to point (27) the examiner disagrees for similar reasons as above. Basically, the examiner has already shown above that the suggestion or motivation to combine the references is proper and where the prior art teaches or suggests ALL the claim limitations. As per reasonably expectation of success, of course there is reasonably expectation of success. AAPA has already stated that scalar processors can perform the protocol processing.

28. In the appellant argument, appellant argued with claim 34 that even if Finch discloses a protocol processor performing protocol processing. Finch does not overcome the previously discussed deficiencies of Aoyama and Asano.

As to point (27) the examiner disagrees. The combination of Aoyama, Asano, and Finch teaches all the claimed limitations as discussed in the rejections.

29. In the appellant argument, the appellant argued (29) there is no teaching or suggestion in Finch that it could be combined with the teaching of Aoyama and Asano.

As to point (29) in response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Finch, e.g., col.8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

30. In the appellant argument, the appellant argued (30) that the Examiner has not satisfied the above requirements in rejecting claims 34 and 37-39.

As to point (30) the examiner disagrees with the appellant's arguments. It is noted that motivation is clearly expressed in the rejections. Clearly a reasonable expectation of success exists. And "All" the claimed limitations have been met as discussed in the rejections.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Denise Tran

Conferees

James Peikari
PPA 2186

Matthew Kim
SPE 2186

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265